IN THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) An integrated circuit comprising:

a power supply I/O pad;

an I/O pad of a first type made of a deposited conductor, ~~wherein each of the power supply I/O and I/O pads has a pad area allocated for it, wherein the power supply I/O pad occupies its allocated pad area but the I/O pad occupies less than its allocated pad area, and~~ wherein the I/O pad of the first type is connected to a first point on ~~an~~ the integrated circuit; and

a strip of deposited conductor located alongside the I/O pad of the ~~fist~~ first type ~~in an unoccupied part of its allocated pad area~~, wherein the strip is connected to a second point on the integrated circuit~~, and~~;

wherein the I/O pad of the first type is narrower than the power supply I/O pad in order to make room for the strip.

2. (Previously Presented) The integrated circuit of claim 1, wherein the I/O pad of the first type is a data I/O pad or a multi-level voltage I/O pad.

3. (Original) The integrated circuit of claim 1, wherein the first point on the integrated circuit is further connected to a circuitry.

4. (Original) The integrated circuit of claim 1, wherein the first point on the integrated circuit is further connected to a power bus.

5. (Original) The integrated circuit of claim 1, wherein the second point on the integrated circuit is further connected to a circuitry.

6. (Original) The integrated circuit of claim 1, wherein the second point on the integrated circuit is further connected to a power bus.

7. (Previously Presented) The integrated circuit of claim 1, wherein the strip is connected to a third point on the integrated circuit.

8. (Original) The integrated circuit of claim 7, wherein the second and third points on the integrated circuit are connected to a circuitry.

9. (Original) The integrated circuit of claim 7, wherein the second and third points on the integrated circuit are connected to a power bus.

10. (Currently Amended) The integrated circuit of claim 1, further comprising:

an I/O pad of a second type made of a deposited conductor ~~and occupying an area smaller than its allocated pad area in order to make room for another strip~~, wherein the I/O pad of the second type is connected to a third point on the integrated circuit; and

a second strip of deposited conductor, wherein the second strip is located alongside the I/O pad of the second type, and wherein the second strip is connected to a fourth point on the integrated circuit;

wherein the I/O pad of the second type is narrower than the power supply I/O pad in order to make room for the second strip.

11. (Previously Presented) The integrated circuit of claim 10, wherein the I/O pad of the second type is a data I/O pad or a multi-level voltage I/O pad.

12. (Original) The integrated circuit of claim 10, wherein the third point on the integrated circuit is further connected to a circuitry.

13. (Original) The integrated circuit of claim 10, wherein the third point on the integrated circuit is further connected to a power bus.

14. (Currently Amended) The integrated circuit of claim [[10]] 1, ~~wherein the other~~ further comprising a second strip of deposited conductor located alongside the I/O pad of the first type, ~~is connected to a fourth point on the integrated circuit~~ wherein the second strip is connected to a third point on the integrated circuit, and wherein the I/O pad of the first type is narrower than the power supply I/O pad in order to make room for the strips of deposited conductor.

15. (Original) The integrated circuit of claim 14, wherein the second, third and fourth points on the integrated circuit are connected to a circuitry.

16. (Original) The integrated circuit of claim 14, wherein the second, third and fourth points on the integrated circuit are connected to a power bus.

17. (Previously Presented) The integrated circuit of claim 1, wherein the I/O pad of the first type provides data or a voltage level to a core circuitry.

18. (Previously Presented) The integrated circuit of claim 4, wherein the power bus is configured as an intersecting grid of a deposited conductor.

19. (Original) The integrated circuit of claim 18, wherein the integrated circuit is comprised of multiple metal layers, and wherein the I/O pad of the first type and the power bus are deposited on different layers.

20. (Original) The integrated circuit of claim 19, wherein the power bus exists at a lowest layer.

21. (Original) The integrated circuit of claim 19, wherein the power bus exists at a second to lowest layer.

22-33 (Cancelled)

34. (Currently Amended) An integrated circuit comprising:

a positive power supply I/O pad made of a deposited conductor;

a positive power bus connected to the positive power supply I/O pad;

a negative power supply I/O pad made of a deposited conductor;

a negative power bus connected to the negative power supply I/O pad;

~~a data or multi-level voltage~~ an I/O pad made of a deposited conductor~~, wherein each of the positive and negative power supply I/O pads and data or multi-level voltage I/O pads has a pad area allocated for it, wherein each of the positive and negative power supply I/O pads occupies its allocated pad area but the data or multi-level voltage I/O pad occupies less than its allocated pad area~~;

~~circuitry connected to the data or multi-level voltage I/O pad;~~

a first strip of deposited conductor located alongside the ~~data or multi-level voltage~~ I/O pad ~~in an unoccupied part of its allocated pad area~~, wherein the first strip is connected to multiple points on the positive power bus; and

a second strip of deposited conductor located alongside the ~~data or multi-level voltage~~ I/O pad, wherein the second strip is connected to multiple points on the negative power bus~~, and~~;

wherein the ~~data or multi-level voltage~~ I/O pad is narrower than the power supply I/O ~~pad~~ pads in order to make room for the first and second strips, respectively.

35. (Original) The integrated circuit of claim 34, wherein the power buses provide positive and negative power to a core circuitry.

36. (Original) The integrated circuit of claim 34, wherein the power buses are configured as intersecting grids of a deposited conductor.

37. (Original) The integrated circuit of claim 34, wherein the integrated circuit is comprised of multiple metal layers, and wherein the positive and negative power buses are deposited on third and fourth layers, respectively.

38. (Currently amended) The integrated circuit of claim 34, wherein the integrated circuit is comprised of multiple metal layers, and wherein the positive and negative power supply I/O pads are deposited on a first layer and a second layer, respectively.

39. (Currently amended) The integrated circuit of claim [[38]] 34, wherein ~~the first and second layers are the same layer~~ the I/O pad is a data I/O pad or a multi-level voltage I/O pad.

40. (Original) The integrated circuit of claim 38, wherein the negative power bus exists at the lowest layer.

41. (Original) The integrated circuit of claim 38, wherein the positive power bus exists at the lowest layer.

42. (Original) The integrated circuit of claim 38, wherein the negative power bus exists at the second lowest layer.

43. (Currently amended) The integrated circuit of claim 38, wherein the negative and positive power buses are further deposited on a fifth layer and a sixth layer, respectively.

44. (Original) The integrated circuit of claim 38, wherein the positive power bus exists at the second lowest layer.

45. (Currently amended) The integrated circuit of claim [[44]] 38, wherein the negative power bus exists at the third lowest layer.

46. (Currently amended) The integrated circuit of claim [[44]] 38, wherein the positive power bus exists at the third lowest layer.

47. (Currently amended) The integrated circuit of claim [[44]] 38, wherein the negative power bus exists at the fourth lowest layer.

48. (Currently amended) The integrated circuit of claim [[44]] 38, wherein the positive power bus exists at the fourth lowest layer.

49. (Currently Amended) The integrated circuit of ~~claims~~ claim 6, wherein the power bus is configured as an intersecting grid of a deposited conductor.

50. (Currently Amended) The integrated circuit of ~~claims~~ claim 9, wherein the power bus is configured as an intersecting grid of a deposited conductor.

51. (Currently Amended) The integrated circuit of ~~claims 13~~ claim 34, wherein ~~the power bus is configured as an intersecting grid of a deposited conductor~~ the I/O pad is configured to provide data or a voltage level to a core circuitry.

52. (Currently Amended) The integrated circuit of ~~claims~~ claim 16, wherein the power bus is configured as an intersecting grid of a deposited conductor.

53. (Currently Amended) A method for configuring an integrated circuit, comprising:

forming core logic on an integrated circuit;

forming on the integrated circuit one or more power buses ~~for carrying~~ configured to carry power to at least one part of the core logic;

allocating a pad area on the integrated circuit for each of a plurality of pads which include at least one or more power pads ~~for supplying~~ configured to supply power to the power buses and one or more I/O (input/output) pads ~~for connection~~ configured to connect to one or more other parts of the core logic;

forming on the integrated circuit the plurality of pads ~~of which each power pad is configured to substantially occupy the pad area allocated for it and each I/O pad is configured to occupy less than the pad area allocated for it so as to leave an unoccupied pad area~~;

forming a plurality of conductive strips, each conductive strip being formed ~~in a designated one of the unoccupied pad areas~~ alongside an I/O pad;

forming in the integrated circuit a plurality of connection pins, a number of which being used for external connections to the power pads, wherein, at least in pairs, the conductive strips are configured to provide parallel connections between power buses of like power so as to avoid increasing the number of connection pins needed for external connections to the power pads.

54. (Previously Presented) A method as in claim 53, wherein each I/O pad is configured as a data I/O pad or a multi-level voltage I/O pad.

55. (Previously Presented) A method as in claim 53, wherein the power is either positive or negative and each of the plurality of power buses is configured as a positive power bus or a negative power bus.

56. (Previously Presented) A method as in claim 53, wherein the power buses are formed to have a grid-type configuration in which they intersect at or near the center of the core logic.

57. (New) An integrated circuit comprising:

a power supply I/O pad;

an I/O pad of a first type, wherein the I/O pad of the first type is connected to a first point on the integrated circuit, wherein the I/O pad of the first type comprises:

a deposited conductor forming a metal contact; and

a strip of deposited conductor, wherein the strip is connected to a second point on the integrated circuit;

wherein the deposited conductor forming the metal contact is narrower than the power supply I/O pad in order to make room for the strip of deposited conductor.

58. (New) The integrated circuit of claim 57, wherein the I/O pad of the first type is a data I/O pad or a multi-level voltage I/O pad.

59. (New) The integrated circuit of claim 57, wherein the strip of deposited conductor is positioned on an outer portion of the I/O pad.

60. (New) The integrated circuit of claim 57, wherein:

the deposited conductor forming the metal contact is positioned on an inner portion of the I/O pad; and

the strip of deposited conductor is positioned on an outer portion of the I/O pad.

61. (New) The integrated circuit of claim 57, wherein the I/O pad further comprises a second strip of deposited conductor, wherein the second strip is connected to a third point on the integrated circuit.

62. (New) The integrated circuit of claim 57, wherein the strip of deposited conductor is connected to a power bus, wherein the power bus is configured to provide power to a core circuitry of the integrated circuit.

63. (New) An integrated circuit comprising:

a power supply I/O pad;

a pad comprising at least a first portion and a second portion, wherein the first portion of the pad includes an I/O pad of a first type made of a deposited conductor, wherein the I/O pad of the first type is connected to a first point on the integrated circuit; and

wherein the second portion of the pad includes a strip of deposited conductor, wherein the strip is located alongside the I/O pad of the first type, wherein the strip is connected to a second point on the integrated circuit, and wherein the I/O pad of the first type is narrower than the power supply I/O pad in order to make room for the strip.

64. (New) The integrated circuit of claim 63, wherein the I/O pad of the first type is a data I/O pad or a multi-level voltage I/O pad.

65. (New) The integrated circuit of claim 63, wherein the strip of deposited conductor is positioned on an outer portion of the pad.

66. (New) The integrated circuit of claim 63, wherein:

the I/O pad of the first type is positioned on an inner portion of the pad; and

the strip of deposited conductor is positioned on an outer portion of the pad.

67. (New) The integrated circuit of claim 63, wherein the pad further comprises a third portion, wherein the third portion of the pad includes a second strip of deposited conductor, wherein the second strip is located alongside the I/O pad of the first type, wherein the second strip is connected to a third point on the integrated circuit.

68. (New) The integrated circuit of claim 63, wherein the strip of deposited conductor is connected to a power bus, wherein the power bus is configured to provide power to a core circuitry of the integrated circuit.